R E M A R K S

Reconsideration of this application, as amended, is respectfully requested.

THE TITLE

The title has been amended to more clearly indicate the nature of the invention to which the claims are directed, as required by the Examiner.

THE CLAIMS

Claims 12 and 22 have been canceled, without prejudice, and independent claims 1 and 14 have been amended to incorporate the features of claims 12 and 22, respectively, and to clarify the features of the present invention.

In addition, each of claims 2-11, 13, 15-21 and 23-25 respectively depending from amended independent claims 1 and 14 have also been amended to clarify the features of the present invention.

More specifically, claims 1 and 14 have been amended to recite the features of the semiconductor device and method of forming same of the present invention whereby a semiconductor substrate is provided which includes a circuit element-forming region (in which an integrated circuit is formed) and a plurality of connection pads; an organic insulating film is formed on the circuit element-forming region; columnar electrodes (for connection to external terminals) are each electrically connected

to at least one of the connection pads; at least one thin film passive element including at least one conductive layer is formed on the insulating film; and a sealing film is provided between the columnar electrodes and covering the at least one thin film passive element and from which an upper edge surface of each of the columnar electrodes is exposed.

In other words, the semiconductor device of the present invention comprises a thin film passive element formed through an organic insulating film on a circuit element-forming region in which an integrated circuit is formed, a sealing film covering the thin film passive element, and columnar electrodes whose upper edge surfaces are exposed from the sealing film.

Claims 4 and 17, moreover, have been amended to recite the embodiment of the present invention whereby the at least one conductive layer of the thin film passive element(s) include at least two portions formed in one layer on the insulating film, and a dielectric material layer is formed in a clearance between the at least two portions. (See, for example, Fig. 16.)

Claims 5 and 18 have been amended to recite the embodiment of the present invention whereby the at least one conductive layer of the thin film passive element(s) include at least two portions formed in one layer on the insulating film, the columnar electrodes are formed as plate-like electrodes respectively positioned on the at least two portions, and a dielectric material layer is formed in a clearance between surfaces of the plate-like electrodes. (See, for example, Fig. 24.)

And claims 7 and 9-11 and 20 and 23-25 have been amended to recite the features of the present invention whereby the inductance element (L) of the thin film passive element(s) comprises at least two terminals respectively connected to one of the connection pads and/or columnar electrodes. (See, for example, Fig. 35A.)

No new matter has been added, and no new issues with respect to patentability have been raised.

Accordingly, it is respectfully requested that the amendments to the claims be approved and entered.

THE PRIOR ART REJECTION

Claims 1-25 were all rejected under either 35 USC 102 or 35 USC 103 as being anticipated by USP 6,180,976 ("Roy") or as being obvious in view of the combination of Roy and one or both of USP 6,002,161 ("Yamazaki") and USP 6,331, 722 ("Yamazaki et al"). These rejections, however, are respectfully traversed with respect to the claims as amended hereinabove.

Roy discloses a semiconductor device comprising a capacitor 400 formed to comprise a top plate 402 and a bottom plate 404 which sandwich a dielectric material on an insulating film 26 on a semiconductor wafer substrate, conductor plugs 414, 416 and 418, wiring lines 408, 410 and 412 connected to the conductor plugs, respectively, and an insulating layer 406 provided between the conductor plugs and the wiring lines to cover the capacitor 400, as shown in FIG. 12. The conductor plugs 414 and 416 are

connected to conductive layers of the upper plate 402 and lower plate 404 of the capacitor 400.

In Roy, the conductor plugs and the wiring lines are connected to components on the semiconductor wafer, but there is no teaching or suggestion in Roy that the conductor plugs and wiring lines are connected to external terminals. In other words, the capacitor of Roy is merely connected to the components formed on the semiconductor wafer. And it is also noted that the insulating film in Roy is a silicon oxide film.

By contrast, according to the structure of the present invention as recited in amended claims 1 and 14, the thin film passive element(s) are formed on the circuit element-forming region in which the integrated circuit is formed. For this reason, the organic insulating film is formed on the circuit element-forming region and the thin film passive element(s) are further formed on the organic insulating film. And it is respectfully submitted that this structure is clearly different from the structure of the capacitor of Roy.

In addition, as pointed out above, the conductor plugs of Roy are merely used to connect to the components on the wafer through the wiring lines, but are not used for connection to external terminals. And in this connection, it is noted that the upper edge surfaces of the conductor plugs of Roy are not exposed to the outside. By contrast, the columnar electrodes of the present invention are provided for connection to external

terminals and the upper edge surfaces of the columnar electrodes are exposed to the outside.

Still further, it is respectfully pointed out that the insulating layer of Roy (which is provided between the conductor plugs to cover the capacitor) clearly does not correspond to the sealing film of the present invention since the conductor plugs of Roy do not correspond to the columnar electrodes of the claimed present invention.

In view of the foregoing, it is respectfully submitted that the structure and method of the present invention as recited in each of amended independent claims 1 and 14 clearly patentably distinguishes over the teachings of Roy.

With respect to amended claims 4, 5, 17 and 18, moreover, it is noted that Roy merely discloses providing a dielectric material layer between the conductive layers of the top plate and bottom plate. The conductive layers sandwiching the dielectric material layer in Roy, however, are not formed in two portions in one layer (as recited in amended claims 4, 5, 17 and 18) nor does Roy disclose, teach or suggest forming the dielectric layer between plate-like electrodes (as recited in amended claims 5 and 18). Accordingly, it is respectfully submitted that the structure and method of the present invention as recited in amended claims 4, 5, 17 and 18 also clearly patentably distinguishes over the teachings of Roy.

Still further, with respect to amended claims 7 and 9-11 and 20 and 23-25, it is respectfully submitted that neither Roy nor

Yamazaki discloses, teaches or suggest the structures recited therein whereby at least two terminals are respectively connected to one of connection pads and/or columnar electrodes. As discussed above, Roy merely concerned with the structure of the integrated circuit formed on the semiconductor wafer. And thus, the structure of the inductance element of the claimed present invention is not at all suggested by the combination of Roy and Yamazaki.

And finally, with respect to claims 8 and 21, it is noted that although Yamazaki et al discloses a laminated element comprising a magnetic material, in Yamazaki et al the specific structure of the magnetic material in the laminated element is not disclosed. Thus, the formation of the magnetic film on the conductive layer of the inductance element as recited in claims 8 and 21 is simply not suggested in Yamazaki et al.

In view of the foregoing, it is respectfully submitted that the present invention as recited in each of amended claims 1-11, 13-21 and 23-25 clearly patentably distinguishes over the teachings of Roy, Yamazaki and Yamazaki et al, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

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Entry of this Amendment, allowance of the claims, and the passing of the application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1-11, 13-21 and 23-25 have been amended as follows:

1. (Amended) A semiconductor device [,] comprising:

a semiconductor substrate including a circuit element-forming region in which an integrated circuit is formed, and a plurality of connection pads;

an organic insulating film formed on said circuit element-forming region;

a plurality of columnar [electrode] electrodes which are provided for connection to external terminals, and which are each electrically connected to at least one of said [plural] plurality of connection pads; [and]

at least one thin film passive element including at least one conductive layer formed on said insulating film; and

a sealing film which is provided between the columnar electrodes and covers the at least one thin film passive element, and from which an upper edge surface of each of the columnar electrodes is exposed.

2. (Amended) The semiconductor device according to claim 1, wherein said thin film passive element [is] comprises at least one capacitance element.

3. (Amended) The semiconductor device according to claim 2, wherein:

said capacitance element includes two conductive layers and a dielectric material layer,

said two conductive layers are stacked one upon the other on said insulating film, and

said dielectric material layer is interposed between the conductive layers.

4. (Amended) The semiconductor device according to claim 2, wherein:

said at least one conductive layer of said capacitance element includes at least two [conductive layers] portions formed in one layer on said insulating film, and

a dielectric material layer [, said two conductive layers positioned apart from each other on said insulating film, and said dielectric layer] is formed in [the] a clearance between the at least two [adjacent] portions [conductive layer].

5. (Amended) The semiconductor device according to claim 2, wherein:

said at least one conductive layer of said capacitance element includes at least two [conductive layers] portions formed in one layer on said insulating film, [and a dielectric material

layer, said two conductive layers positioned adjacent to and apart from each other on said insulating film and]

said columnar electrodes are formed as plate-like electrodes respectively positioned on the [conductor layers] at least two portions, and

[said] a dielectric material layer is formed in [the] a clearance between [one end the opposite ends of the adjacent] surfaces of the plate-like electrodes.

6. (Amended) The semiconductor device according to claim 1, wherein said thin film passive element [is] comprises at least one inductance element.

7. (Amended) The semiconductor device according to claim 6, wherein:

said inductance element includes one conductive layer [, said conductive layer is formed in the shape of any] having one of an angular eddy shape, a rectangular wave shape, and a loop shape,

said connection pads include at least one first connection pad that is not electrically connected to any of said columnar electrodes, and at least one second connection pad electrically connected to at least one of said columnar electrodes, and

said inductance element includes at least two terminals, at least one of which is connected to at least one of said first connection pad and said second connection pad.

8. (Amended) The semiconductor device according to claim 7, wherein said inductance element further comprises a magnetic film formed on said one conductive layer.

9. (Amended) The semiconductor device according to claim 1, wherein said thin film passive element includes at least two [terminal electrodes] terminals, at least one of [said two terminal electrodes of said thin film passive element being] which is electrically connected to one of said columnar [electrode] electrodes.

10. (Amended) The semiconductor device according to claim 1, wherein said thin film passive element includes at least two [terminal electrodes] terminals, at least one of [said two terminal electrodes of said thin film passive element being] which is electrically connected to one of said connection [pad] pads.

11. (Amended) The semiconductor device according to claim 1, wherein said thin film passive element includes at least two [terminal electrodes] terminals, each of [said terminal electrodes of said thin film passive element being] which is electrically connected to at least one of said connection [pad] pads and said columnar [electrode] electrodes.

13. (Amended) The semiconductor device according to claim 1, [which further includes a plurality of] wherein said at least one thin film passive comprises a plurality of thin film passive elements.

14. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer substrate including a plurality of chip forming regions each having a circuit element-forming region in which an integrated circuit is formed, and a plurality of connection pads;

forming an organic insulating film on the circuit element-forming region of each of said chip forming regions;

[forming at least one thin film passive element including at least one conductive layer on said insulating film;]

forming a plurality of columnar [electrode] electrodes which are provided for connection to an external terminals, and which are each electrically connected to at least one of said [plural] plurality of connection pads; [and]

forming a plurality of thin film passive elements each including at least one conductive layer on said insulating film;

forming a sealing film on the semiconductor wafer substrate between the columnar electrodes and covering the thin film passive elements and the columnar electrodes;

exposing an upper edge surface of each of the columnar electrodes from the sealing film; and

dividing said semiconductor wafer substrate into individual chip forming regions so as to form a plurality of semiconductor devices each having at least one of said thin film passive [element] elements.

15. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein said forming of said thin film passive [element] elements comprises forming at least one [of forming a] capacitance element.

16. (Amended) The method of manufacturing a semiconductor device according to claim 15, wherein said forming of [a] each said capacitance element comprises:

forming a first conductive layer on the circuit element-forming region of said semiconductor substrate [with an insulating film interposed therebetween];

forming a dielectric material layer on said first conductive layer; and

forming a second conductive layer on said dielectric material layer.

17. (Amended) The method of manufacturing a semiconductor device according to claim 15, wherein said forming of [the] each said capacitance element comprises:

forming [two pieces of] on said insulating film one conductive layer having at least two portions [positioned

adjacent to each other a predetermined distance apart from each other on said insulating film]; and

forming a dielectric material layer in [the] a clearance between [adjacent] the at least two portions [pieces of said conductive layer].

18. (Amended) The method of manufacturing a semiconductor device according to claim 15, wherein said forming of [the] each said capacitance element comprises:

forming [two pieces of the] on said insulating film one conductive layer having at least two portions [positioned adjacent to each other a predetermined distance apart from each other on said insulating film];

forming said columnar electrodes as [a] plate-like [electrode] electrodes respectively on [each of the two adjacent pieces of said conductive layer] the at least two portions; and

forming a dielectric material layer in [the] a clearance between [one end and the other end] surfaces of said plate-like electrodes.

19. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein said forming of said thin film passive [element] elements comprises forming at least one inductance element.

20. (Amended) The method of manufacturing a semiconductor device according to claim 19, wherein said forming of [the] each said inductance element comprises:

patterning [said] one conductive layer in any [of the shapes selected from the group consisting] one of an angular eddy shape, a rectangular wave shape and a loop shape;

forming said connection pads to include at least one first connection pad that is not electrically connected to any of said columnar electrodes, and at least one second connection pad electrically connected to at least one of said columnar electrodes, and

forming at least two terminals, at least one of which is connected to at least one of said first connection pad and said second connection pad.

21. (Amended) The method of manufacturing a semiconductor device according to claim 20, wherein said forming of the inductance element further comprises forming a magnetic film on said one conductive layer.

23. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein said forming of said thin film passive [element] elements comprises forming at least two terminals, at least one of which is electrically connected to one of said columnar electrodes [electrode in at least one of the

electrode terminals at one end and the other end of said thin film passive element].

24. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein said forming of said thin film passive [element] elements comprises forming at least two terminals, at least one of which is electrically connected to one of [connecting at least one of the electrode terminals at one end and the other end of said thin film passive element to] said connection [pad] pads.

25. (Amended) The method of manufacturing a semiconductor device according to claim 14, wherein said forming of said thin film passive [element] elements comprises forming at least two terminals, each of which is electrically connected [connecting each electrode terminal of said thin film passive element] to at least one of said connection [pad] pads and said columnar [electrode] electrodes.